USER'S GUIDE

QUADRASYNC/E

MODEL 10028

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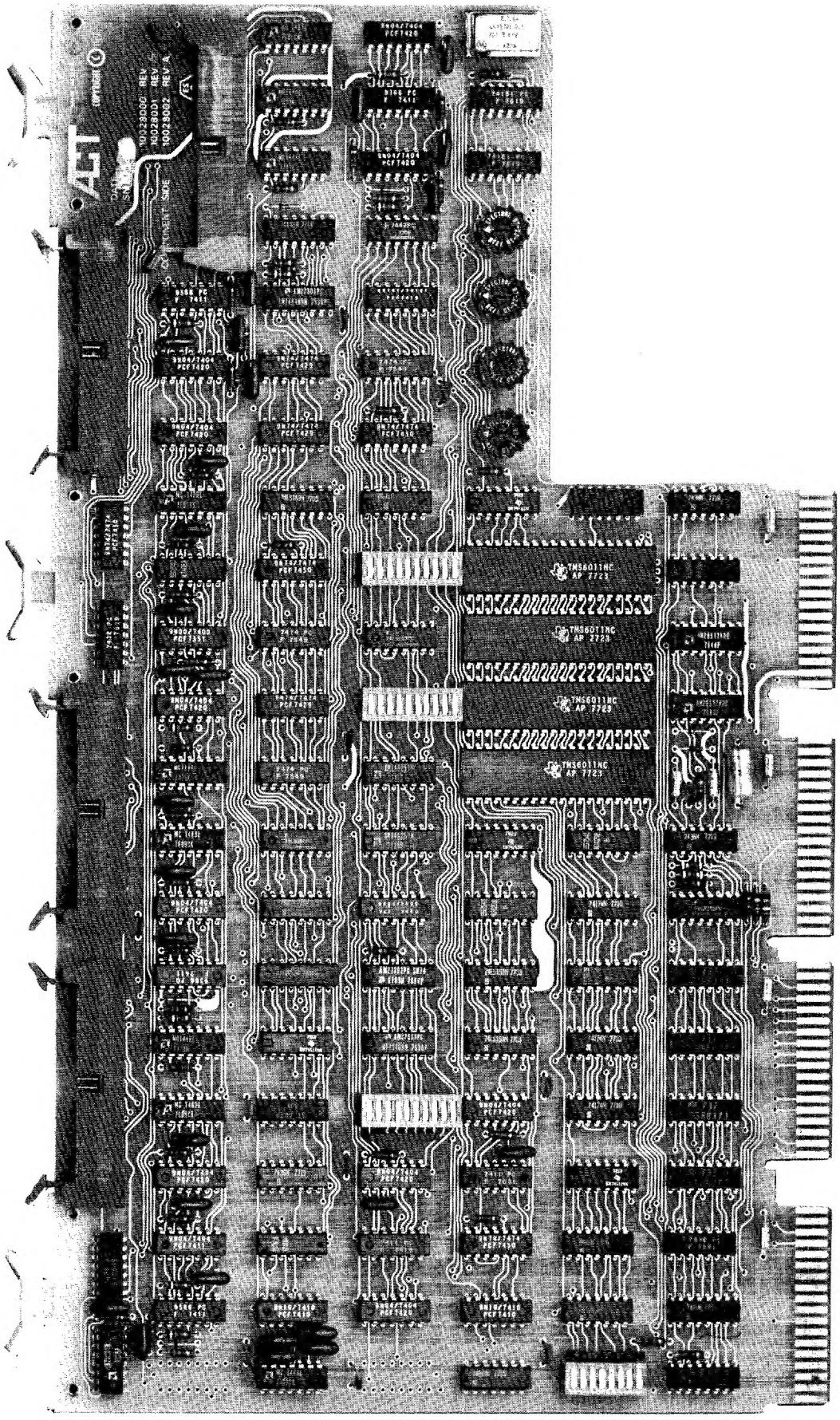


QUADRASYNC/E - MODEL 10028

FUNCTION

Provides an interface between the PDP*-11 Unibus* and four asynchronous EIA Serial Communication Channels with complete dataset control for each channel. System software compatible with the Digital Equipment Corporation DL-11E. (Does not support current Loop or reader enable relay circuit).

MECHANICAL

The QUADRASYNC/E** consists of one quad module which can be installed in any Small Peripheral Controller (SPC) slot.

OPERATING MODE

Full duplex or half duplex communication capability the same as furnished with the DEC* Model DL-11E.

DATA FORMAT

Asynchronous, EIA Serial. One start bit, 8 data bits and one stop bit. Low order bit first. Data bits and stop bits are switch selectable.

BUS LOADING

The QUADRASYNC/E presents one unit load to the Unibus.

ELECTRICAL INTERFACE

The QUADRASYNC/E provides a voltage level interface and on-board connectors whose signal levels conform to Electronic Industries Association Standard RS232C and CCITT Recommendations V.24. The leads supported are:

Protective Ground	Signal Ground	Secondary Transmitted Data
Transmitted Data	Data Terminal Ready	Secondary Received Data
Received Data	Request to Send	
Clear to Send	Carrier	Ring Indicator

Any cable compatible with the DEC DL-11E is compatible with the QUADRASYNC/E.

POWER REQUIREMENTS

2.300 amps @ + 5V
0.100 amps @ + 15V
0.200 amps @ - 15V

BUS REQUEST LEVEL

Level 4 (BG 4)

DATA RATES

The QUADRASYNC/E offers eight independently selectable baud rates for each channel. The transmitter and receiver of each channel operate at the identical baud rate. The baud rates are:

BAUD RATE	SWITCH POSITION
9600 baud	1
4800 baud	2
2400 baud	3
1200 baud	4
600 baud	5
300 baud	6
150 baud	7
75 baud	8

NOTES:

1) Switch position 1 is when the arrow ON switch is pointed directly toward the letter '1' printed on the circuit board.

2) Ascending switch positions are in clockwise direction.

3) CH 1 switch is closest to center of board and ascending to CH 4 on left side of board.

PROGRAMMING SPECIFICATIONS

Receiver Status Register (RCSR): 77XXX0

RCSR

15	14	13	12	11	10	9 8	7	6	5	4	3	2	1	0
R	R	R	R	R	R	N.U.	R	R/W	R/W	N.U.	R/W	R/W	R/W	W

BIT	DESCRIPTION AND OPERATION
15	Dataset status change. Read only. Set by any change in the state of bits 13, 12 or 10 of the RCSR, and by a 'OFF' to 'ON' state of bit 14 of the RCSR. Cleared by INIT and by reading from RCSR.
14	Ring indicator. Read only. This bit follows the state of the RING INDICATOR lead from the dataset. It is set when RING INDICATOR is high and cleared when low.
13	Clear to send. Read only. This bit follows the state of the CLEAR TO SEND lead from the dataset. It is set when CTS is high and cleared when low.
12	Carrier detect. Read only. This bit follows the state of the Received Line Signal Detector (Carrier) lead from the dataset. It is set when carrier is high and cleared when low.
11	Receiver Active. Read only. Read as '0'.(This bit is not functionally used on the QUADRASYNC/E).
10	Secondary Received data. Read only. This bit follows the state of the secondary receive data lead. The bit is set when the signal is high (spacing) and cleared when that signal is low (marking).
9-8	Not Used. Read as '0'.
7	Receiver Done. Read only. Set when the receiver has transferred an incoming character to the receiver data buffer register (RBUF). Cleared by setting bit 0 (reader enable) in RCSR, by addressing RBUF, or by INIT. If bit 6 in RCSR is set, the setting of bit 7 will cause an interrupt request to be generated.
6	Receiver Interrupt Enable. Read/write. This bit, when set, causes an interrupt request to be generated each time bit 7 in RCSR is set. Cleared by INIT or by the program.

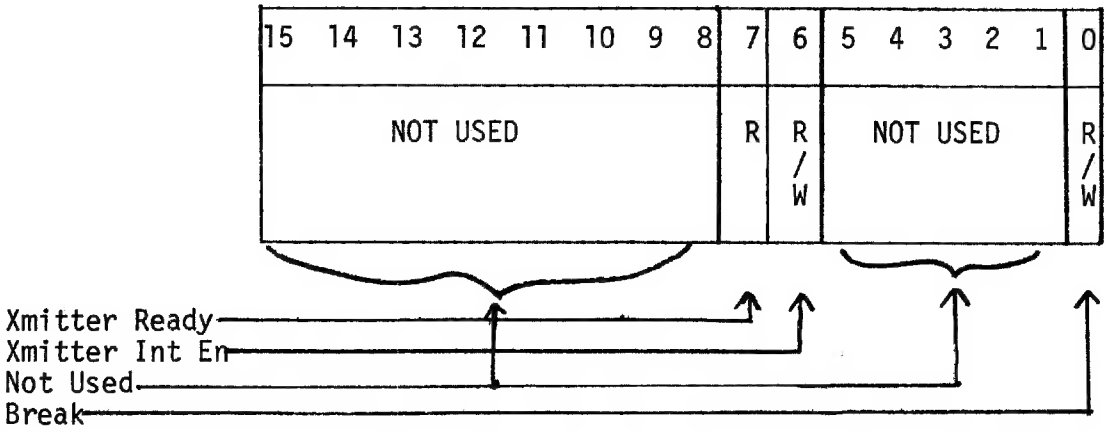
BIT	DESCRIPTION AND OPERATION
5	Dataset Interrupt Enable. Read/write. This bit, when set causes an interrupt request to be generated each time bit 15 in RCSR is set. Cleared by INIT, or by the program.
4	Not Used. Read as '0'.
3	Secondary Transmitted Data. Read/write. This bit, when set causes the secondary transmitted data signal to the dataset to go high (spacing) and when cleared, causes that signal to go low (marking). Cleared by INIT, or by the program.
2	Request to send. Read/write. This bit, when set, causes the Request to Send signal to the dataset to go high, and when cleared, causes that signal to go low. Cleared by INIT, or by the program.
1	Data Terminal Ready. Read/write. This bit, when set, causes the Data Terminal Ready signal to the dataset to go high, and when cleared, causes that signal to go low. Cleared by INIT, or by the program.
0	Reader Enable. Write only. This bit, when set, clears receiver done (bit 7) in RCSR. Automatically cleared. (This bit is not operational for the reader run relay).

Receiver Data Buffer Register (RBUF) 77XXX2

RBUF

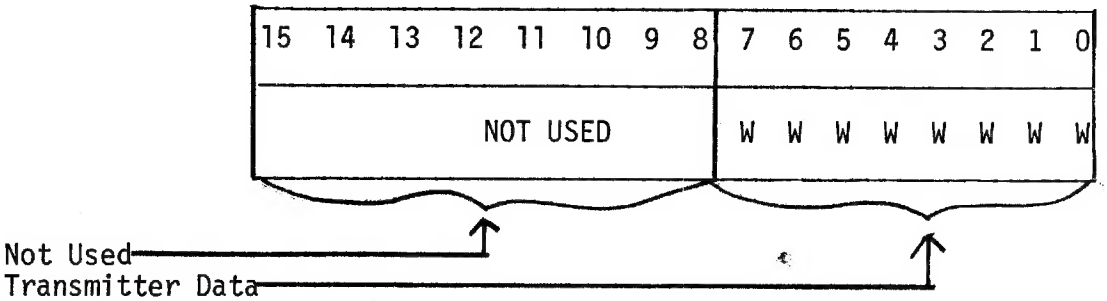
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R	R	R	R	N. U.				R							

BIT	DESCRIPTION AND OPERATION
15	Error. Read only. This bit is set if bit 14, 13, or 12 (any combination) in RBUF is set. Cleared if only the above bits are cleared.
14	Overrun. Read only. This bit set if bit 7 in RCSR is not cleared before the UART attempts to present a new character to RBUF. If the UART attempts to set bit 7 in RCSR, and it is already set, the previous character in RBUF is lost and the new character replaces it.
13	Framing Error. Read only. This bit is set if the UART, at the time it samples the received data line in the center of the first stop bit, finds the line in a spacing (0) condition. This may indicate an open input line, "Break" signal, or excessive distortion of the received character.
12	Received Data Parity Error. Read only. This bit is set if the parity of the received data character does not agree with the parity specified (odd or even). Read as zero if 'no parity check' option is selected.
7-0	Received Data. Read only. Last complete character assembled by the UART, characters are right justified when characters are less than 8 bits.



BIT	DESCRIPTION AND OPERATION
15-8	Not Used. Read as zero.
7	Transmitter Ready. Read only. Set when transmitter can accept another character and by INIT. Cleared when a character is loaded into the transmitter buffer.
6	Transmitter Interrupt Enable. Read/write. When set, will cause an interrupt request whenever bit 7 in the transmitter status is set. Cleared by the program and by INIT.
5-1	Not used. Read as zero.
0	Break. Read/write. This bit when set, clamps the serial data output of the UART transmitter to a spacing (logical 0) condition. Cleared by INIT, and by the program.

Transmitter Buffer Registers: 77XXX6



BIT	DESCRIPTION AND OPERATION
7-0	Write only. Contains the character to be transmitted by the UART. When fewer than 8 data bits, the character must be right justified when loaded into the transmitter buffer. A bit set will cause a mark to appear on the transmitted data lead for one bit time. Cleared by INIT.

FIXED							SWITCH 1								FIXED			REGISTER
							1	2	3	4	5	6	7	8				
17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	0	0	0	R C S R
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	0	1	0	R B U F
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	1	0	0	X C S R
1	1	1	1	1	1	1	X	X	X	X	X	X	X	X	1	1	0	X B U F

5 6 5 0

Address Range: 7 7 7 7 7 6 thru 7 7 4 0 0 0

Address is normally set for: 7 7 5 6 1 0 thru 7 7 5 6 4 6

Address selection selects the beginning address of the 16 contigous address of the Quad/E

SW - OPEN = 0

SW - CLOSED = 1

VECTOR ADDRESS:

SWITCH 8						FIXED			VECTOR
5	6	7	8	9	10				
8	7	6	5	4	3	2	1	0	
X	X	X	X	X	X	0	0	0	RCVR
X	X	X	X	X	X	1	0	0	XMIT

SW-OPEN = 1

SW-CLOSED = 0

310 ‡ 350

Vector address selection selects the beginning vector addresses for the four channels of the Quad/E.

Vector addresses are normally set to 774 thru 740

VECTOR RANGE: 000 through 777

OPERATION WITHOUT MODEM: The QUADRASYNC/E is normally used for operation with a modem. Any or all of the four QUADRASYNC/E channels can be modified for use without modem by using positions 1 through 4 of switch 8. These switches are normally set to the open position which causes the Data Terminal Ready and Request to Send signals to be under program control. For operation without modem, these two signals can be switched to the ON state. For applications with modem on some lines and not on others, a null modem can be used on the no-modem lines. The table below shows the switch settings for each channel. For applications with modem on none of the lines, close all four switches and address the device as a DL11-B.

Switch 8		Description of Setting
Position	Setting	
4	Open	Channel 1 - normal operation with modem
4	Closed	Channel 1 - operation without modem
3	Open	Channel 2 - normal operation with modem
3	Closed	Channel 2 - operation without modem
2	Open	Channel 3 - normal operation with modem
2	Closed	Channel 3 - operation without modem
1	Open	Channel 4 - normal operation with modem
1	Closed	Channel 4 - operation without modem

CONNECTOR LIST

J1

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #1 Signal GND	2
VV	CH #1 Signal GND	1
TT	CH #1 + 5 Vdc	3
DD	CH #1 EIA Term. Rdy	15
V	CH #1 EIA Req to send	23
J	CH #1 EIA Rec Data	33
F	CH #1 EIA Xmit Data	35
FF	CH #1 EIA Sec Xmit Data	13
X	CH #1 EIA Ring Ind.	21
BB	CH #1 EIA Carrier	17
T	CH #1 EIA Clr to Send	25
JJ	CH #1 EIA Sec Rec Data	11

J2

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #2 Signal GND	2
VV	CH #2 Signal GND	1
TT	CH #2 + 5 Vdc	3
DD	CH #2 EIA Term. Rdy	15
V	CH #2 EIA Req to Send	23
J	CH #2 EIA Rec Data	33
F	CH #2 EIA Xmit Data	35
FF	CH #2 EIA Sec Xmit Data	13
X	CH #2 EIA Ring Ind.	21
BB	CH #2 EIA Carrier	17
T	CH #2 EIA Clr to Send	25
JJ	CH #2 EIA Sec Rec Data	11

CONNECTOR LIST

J3

BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #3 Signal Gnd	2
VV	CH #3 Signal Gnd	1
TT	CH #3 + 5 Vdc	3
DD	CH #3 EIA Term. Rdy	15
V	CH #3 EIA Req to Send	23
J	CH #3 EIA Rec Data	33
F	CH #3 EIA Xmit Data	35
FF	CH #3 EIA Sec Xmit Data	13
X	CH #3 EIA Ring Ind.	21
BB	CH #3 EIA Carrier	17
T	CH #3 EIA Clr to Send	25
JJ	CH #3 EIA Sec Rec Data	11

J4

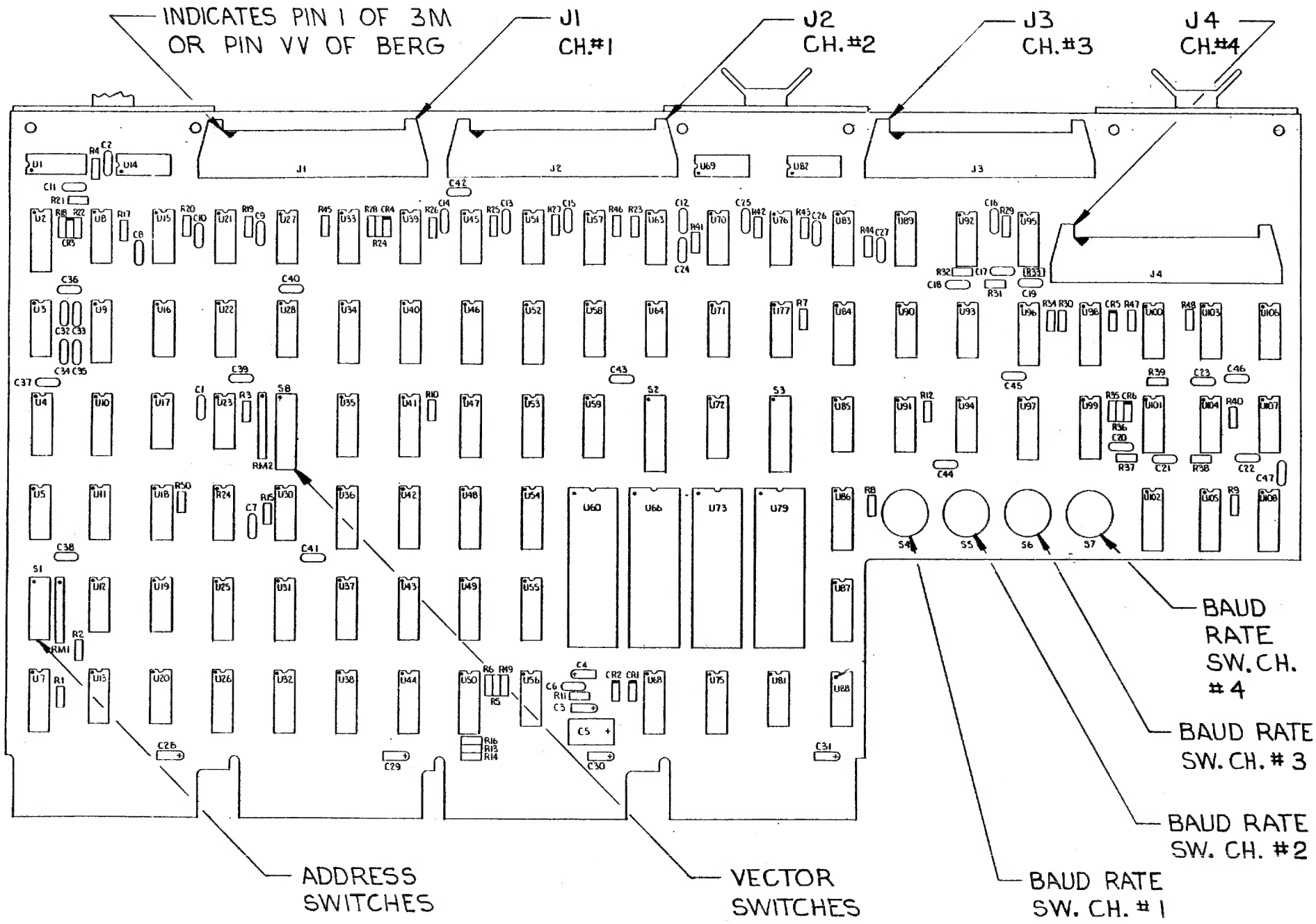
BERG PIN NO.	SIGNAL	3M PIN NO.
UU	CH #4 Signal Gnd	2
VV	CH #4 Signal Gnd	1
TT	CH #4 + 5 Vdc	3
DD	CH #4 EIA Term. Rdy	15
V	CH #4 EIA Req to Send	23
J	CH #4 EIA Rec Data	33
F	CH #4 EIA Xmit Data	35
FF	CH #4 EIA Sec Xmit Data	13
X	CH #4 EIA Ring Ind.	21
BB	CH #4 EIA Carrier	17
T	CH #4 EIA Clr to Send	25
JJ	CH #4 EIA Sec Rec Data	11

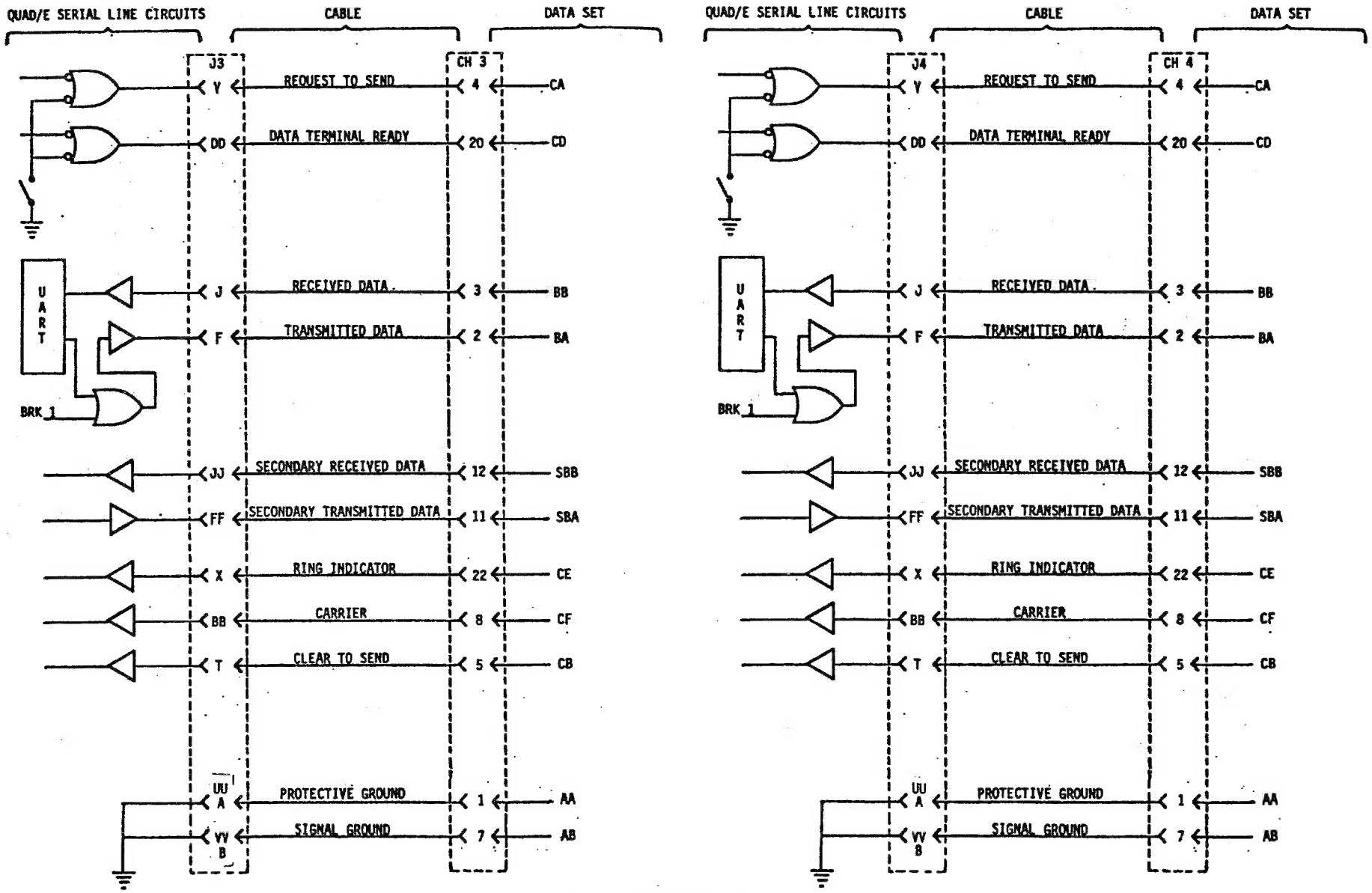
OPTION SELECT:

	PARITY SELECT			
CHANNEL	ENABLED	DISABLED	ODD	EVEN
1	S2-1 CLOSED	S2-1 OPEN	S2-2 CLOSED	S2-2 OPEN
2	S2-6 CLOSED	S2-6 OPEN	S2-7 CLOSED	S2-7 OPEN
3	S3-1 CLOSED	S3-1 OPEN	S3-2 CLOSED	S3-2 OPEN
4	S3-6 CLOSED	S3-6 OPEN	S3-7 CLOSED	S3-7 OPEN

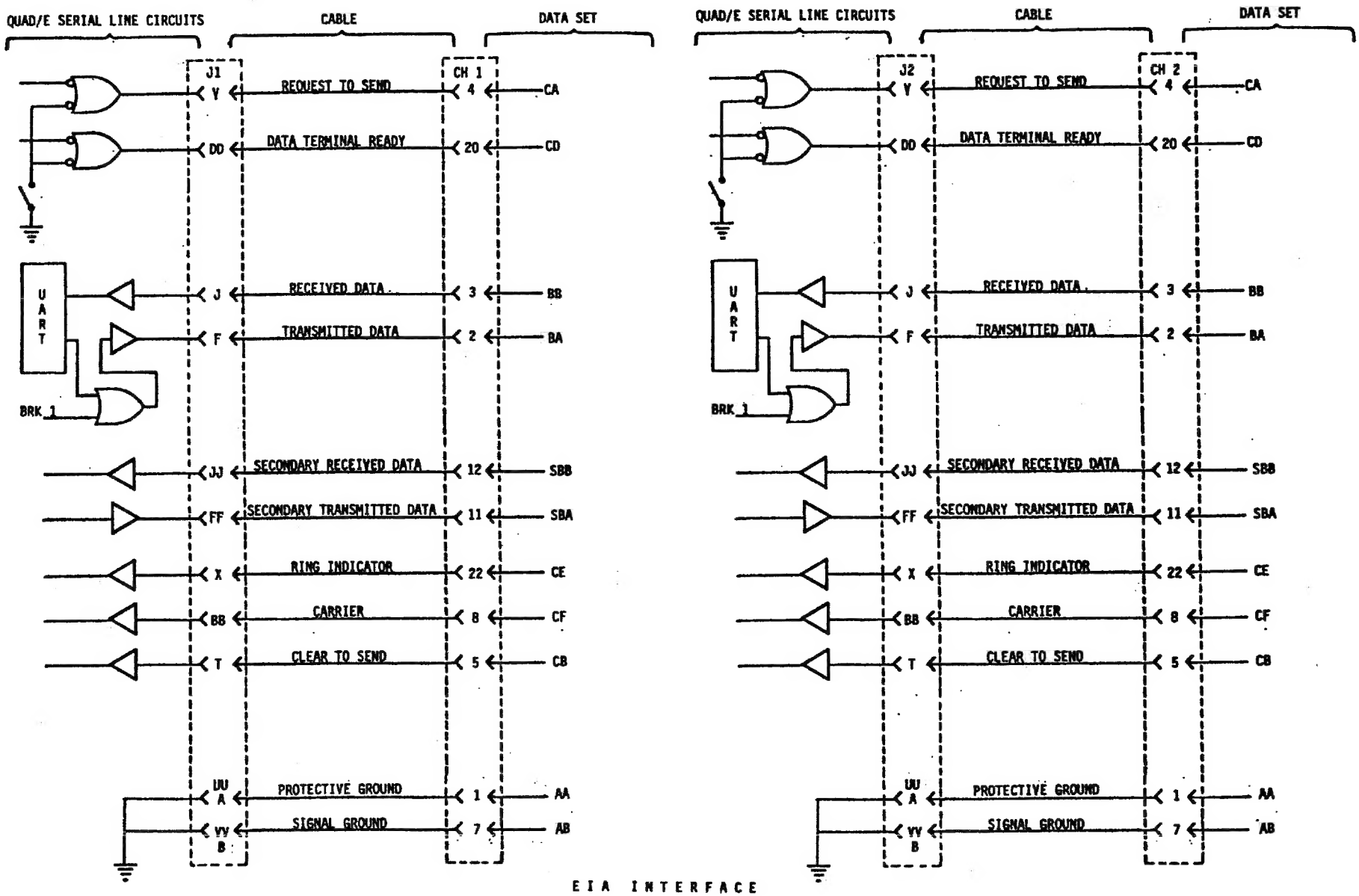
	WORD LENGTH SELECT			
CHANNEL	5 DATA BITS	6 DATA BITS	7 DATA BITS	8 DATA BITS
1	S2-4 CLOSED S2-5 CLOSED	S2-4 CLOSED S2-5 OPEN	S2-4 OPEN S2-5 CLOSED	S2-4 OPEN S2-5 OPEN
2	S2-9 CLOSED S2-10 CLOSED	S2-9 CLOSED S2-10 OPEN	S2-9 OPEN S2-10 CLOSED	S2-9 OPEN S2-10 OPEN
3	S3-4 CLOSED S3-5 CLOSED	S3-4 CLOSED S3-5 OPEN	S3-4 OPEN S3-5 CLOSED	S3-4 OPEN S3-5 OPEN
4	S3-9 CLOSED S3-10 CLOSED	S3-9 CLOSED S3-10 OPEN	S3-9 OPEN S3-10 CLOSED	S3-9 OPEN S3-10 OPEN

	STOP BIT SELECT	
CHANNEL	ONE	TWO
1	S2-3 CLOSED	S2-3 OPEN
2	S2-8 CLOSED	S2-8 OPEN
3	S3-3 CLOSED	S3-3 OPEN
4	S3-8 CLOSED	S3-8 OPEN


INDICATES PIN 1 OF 3M
OR PIN VV OF BERG
J1
CH.#1
J2
CH.#2
J3
CH.#3
J4
CH.#4
BAUD
RATE
SW. CH.
#4
BAUD RATE
SW. CH. #3
BAUD RATE
SW. CH. #2
BAUD RATE
SW. CH. #1
ADDRESS
SWITCHES
VECTOR
SWITCHES



EIA INTERFACE



EIA INTERFACE